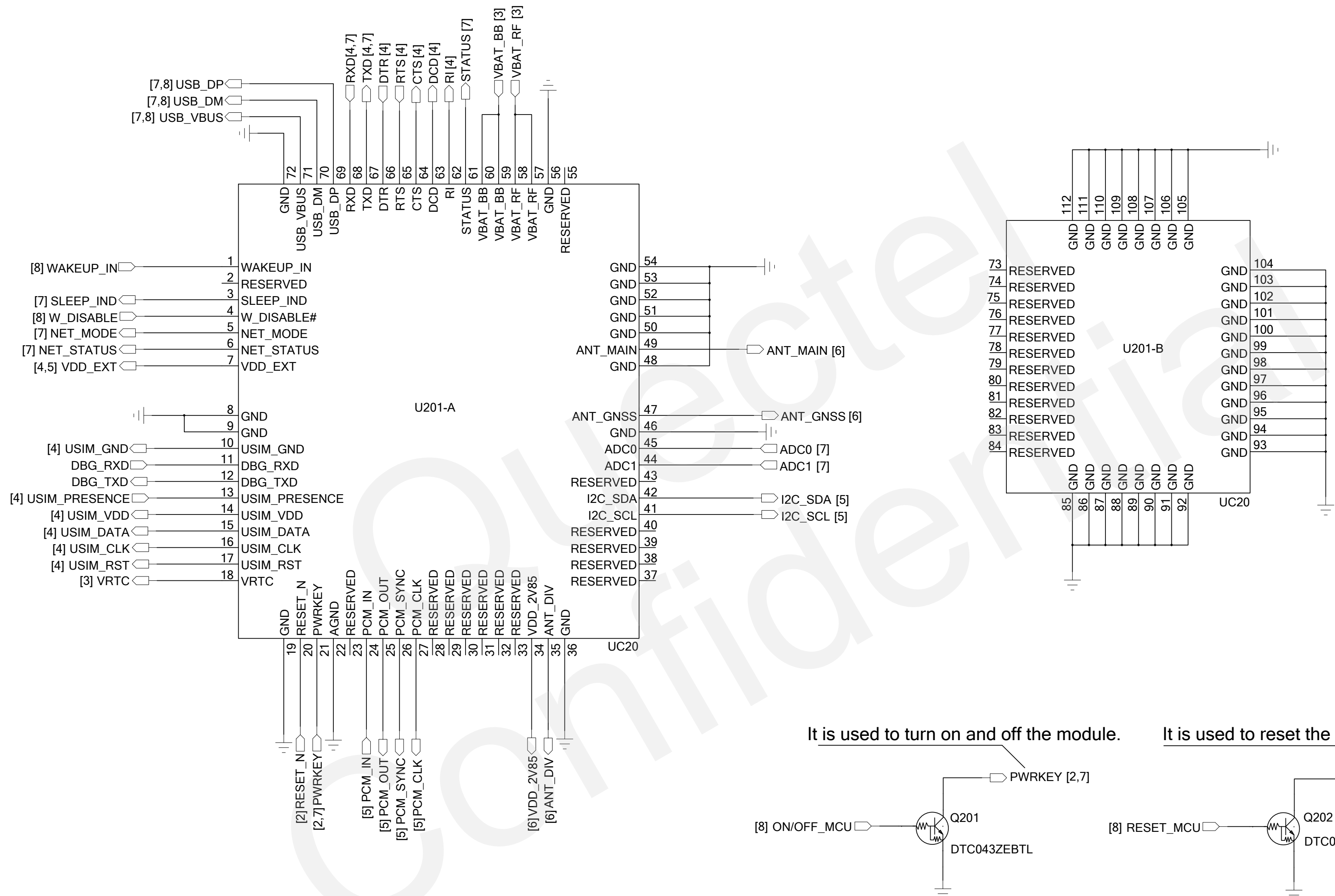


6		5		4		3		2		1																					
UC20 Reference Design Explanation 1. Revision History <table><thead><tr><th>Revision</th><th>Date</th><th>Description</th></tr></thead><tbody><tr><td>V1.01</td><td>2013.05</td><td>Initial.</td></tr><tr><td>V1.02</td><td>2013.07</td><td>1. Updated the name of UC20' Pins 1, 3, 4, 10, 13~17, 34, 47 and 55. 2. Reserved capacitor C801 between USB_DP and USB_DM signal lines. 3. Updated U301 circuit, added R307 and D302. 4. Updated GNSS reference circuit. 5. Updated the description of firmware upgrade and reserved testpoints. 6. Updated ADC voltage range. 7. Added SLEEP_IND, WAKEUP_IN and W_DISABLE# connections, removed the pin connected with Pin 55. 8. Changed R408 from NM to 15K.</td></tr></tbody></table> 2. Index of Reference Design Sheet 1: Design Explanation Sheet 2: Module Interface Sheet 3: Power Supply Design Sheet 4: UART and USIM Design Sheet 5: Audio Design Sheet 6: RF and GNSS Design Sheet 7: Other Designs Sheet 8: MCU Interface <table><thead><tr><th colspan="3">Quectel Wireless Solutions</th></tr></thead><tbody><tr><td>DRAWN BY <Mountain.ZHOU></td><td>PROJECT <UC20 Reference Design></td><td>TITLE <Design Explanation></td></tr><tr><td rowspan="2">CHECKED BY <Bruce.YU></td><td>SIZE A2</td><td>VER 1.02</td></tr><tr><td colspan="2">SHEET 1 of 8 <2013.07></td></tr></tbody></table>												Revision	Date	Description	V1.01	2013.05	Initial.	V1.02	2013.07	1. Updated the name of UC20' Pins 1, 3, 4, 10, 13~17, 34, 47 and 55. 2. Reserved capacitor C801 between USB_DP and USB_DM signal lines. 3. Updated U301 circuit, added R307 and D302. 4. Updated GNSS reference circuit. 5. Updated the description of firmware upgrade and reserved testpoints. 6. Updated ADC voltage range. 7. Added SLEEP_IND, WAKEUP_IN and W_DISABLE# connections, removed the pin connected with Pin 55. 8. Changed R408 from NM to 15K.	Quectel Wireless Solutions			DRAWN BY <Mountain.ZHOU>	PROJECT <UC20 Reference Design>	TITLE <Design Explanation>	CHECKED BY <Bruce.YU>	SIZE A2	VER 1.02	SHEET 1 of 8 <2013.07>	
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Module Interface



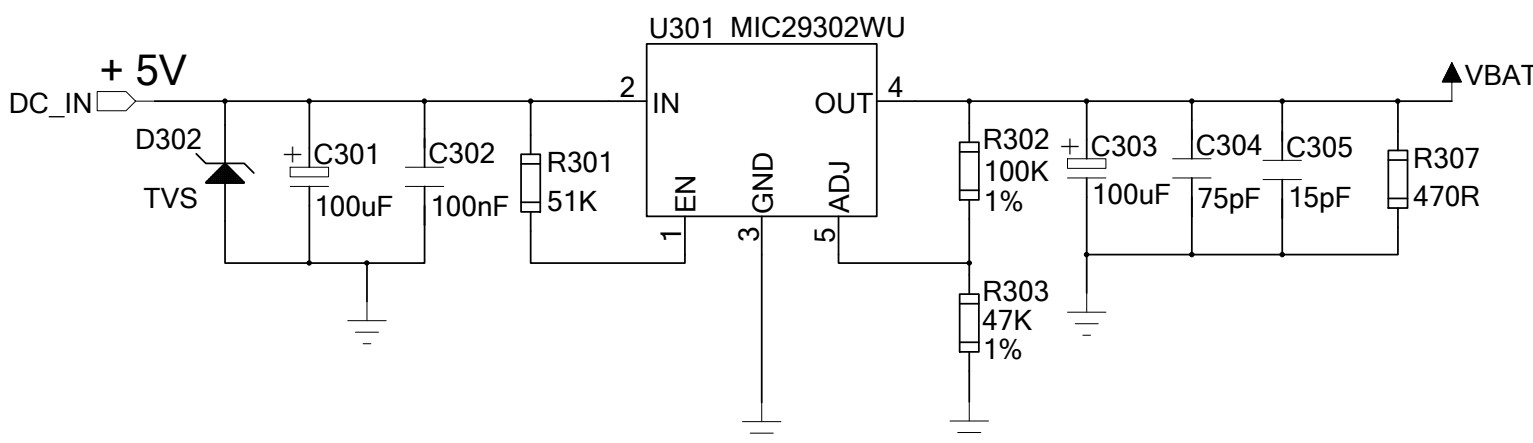
Note:
Keep all reserved pins open.

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Power Supply Design

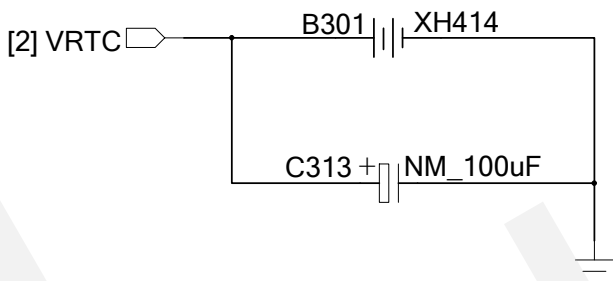
LDO Application

It is used when the input voltage is below 7V.



$$VBAT = (R302/R303+1)*1.24 = 3.88V$$

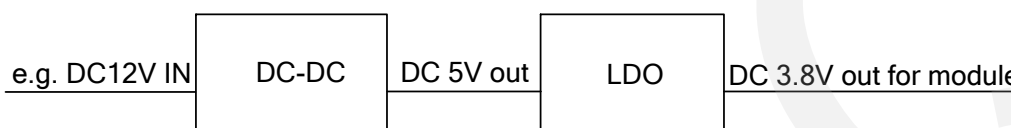
VRTC Design



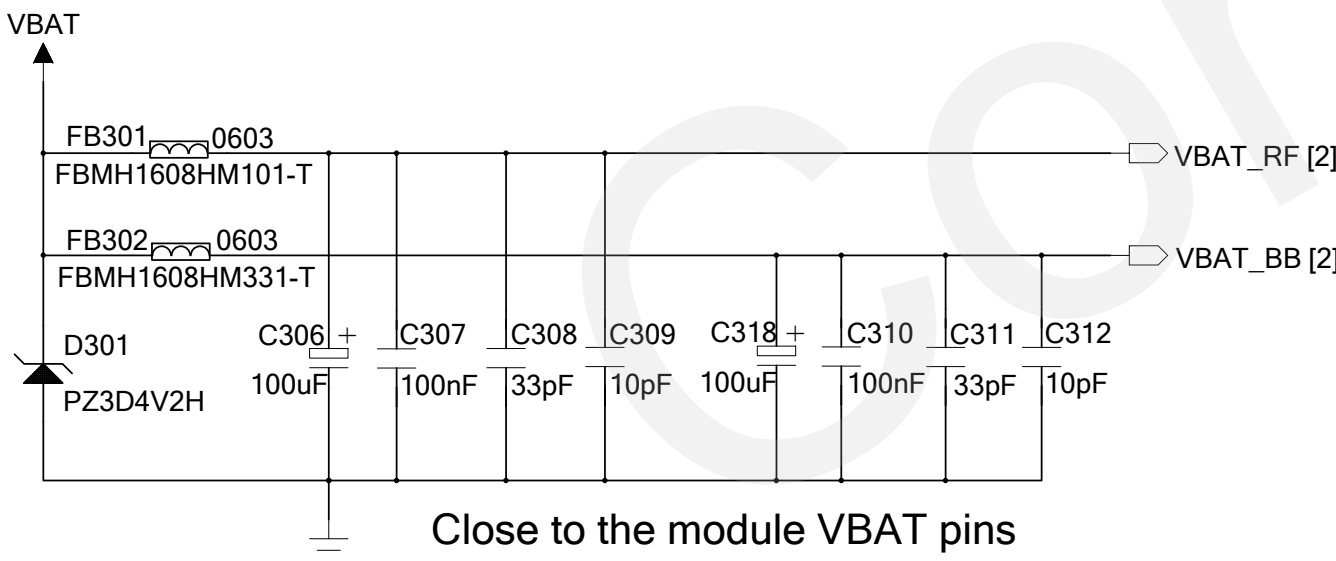
If VRTC function is not used, keep VRTC pin open.

DC-DC Application

1. It is used when the input voltage is above 9V in the vehicle application.
2. Use DC-DC to convert high input voltage to 5V, and LDO will generate 3.8V typical voltage for the module.



VBAT Design

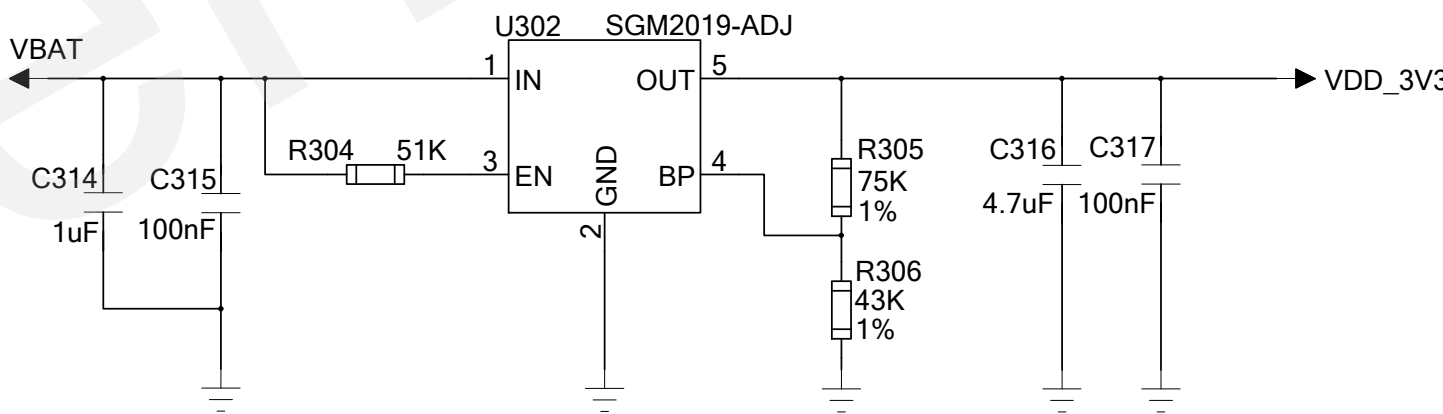


Close to the module VBAT pins

Notes:

1. VBAT should be routed in star mode to VBAT_BB and VBAT_RF net.
2. The rated current of FB301 should be more than 2.0A, and FB302 more than 0.8A.

Supply Power to PCM Codec and ADC Circuit



$$VDD_3V3 = (R305/R306+1)*1.207 = 3.3V$$

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D

C



A

- B

C

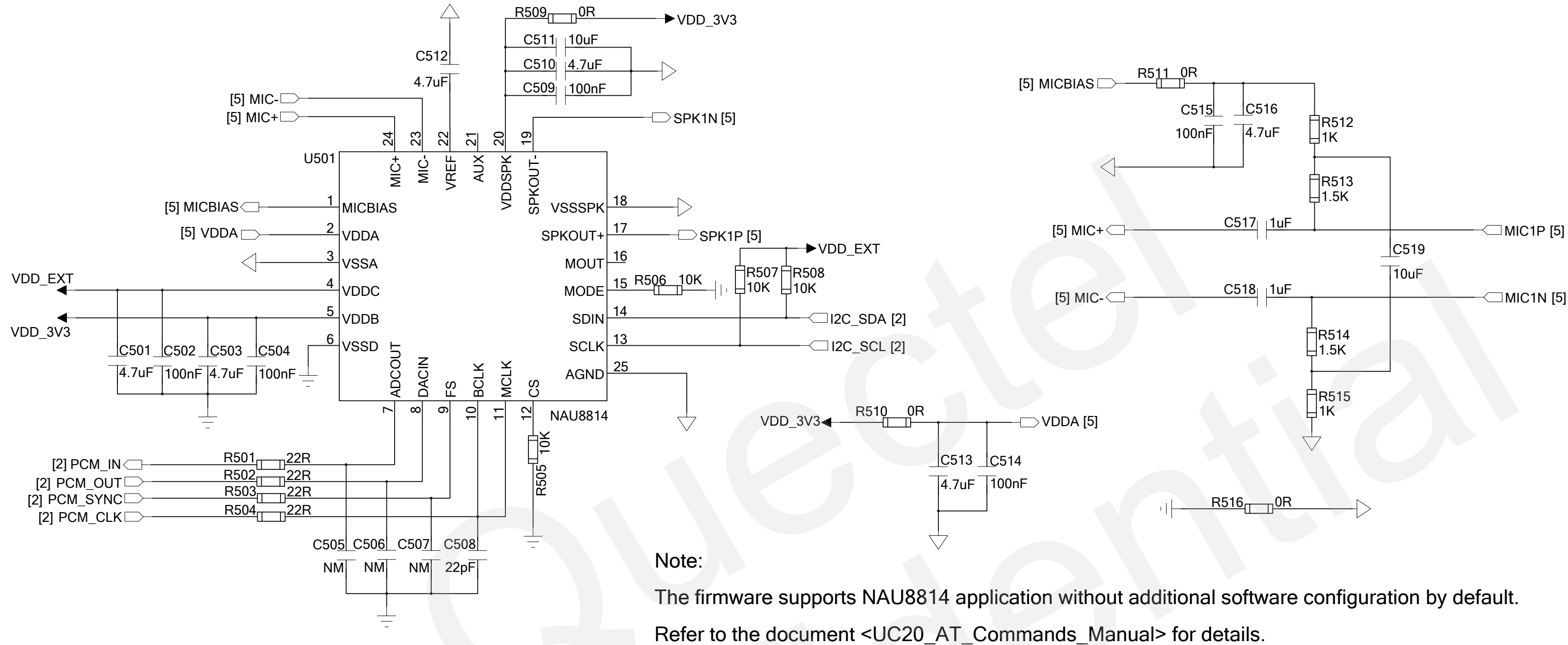


A

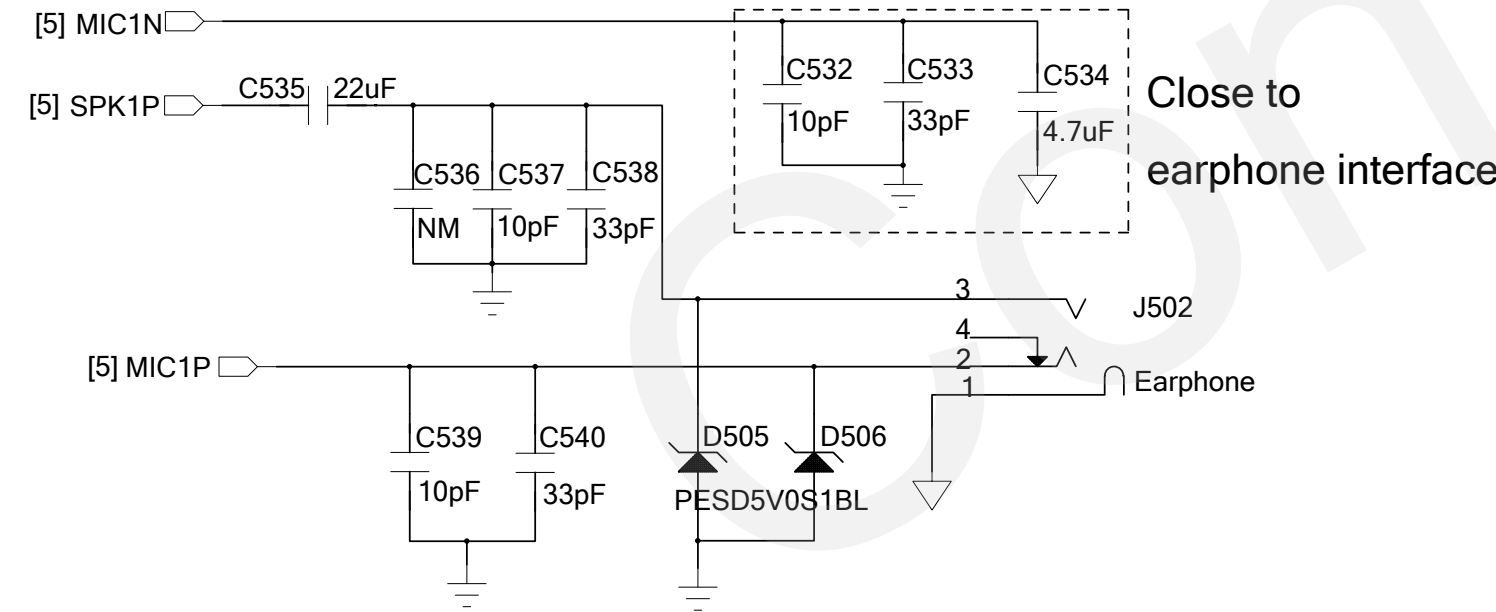
- 1

Audio Design

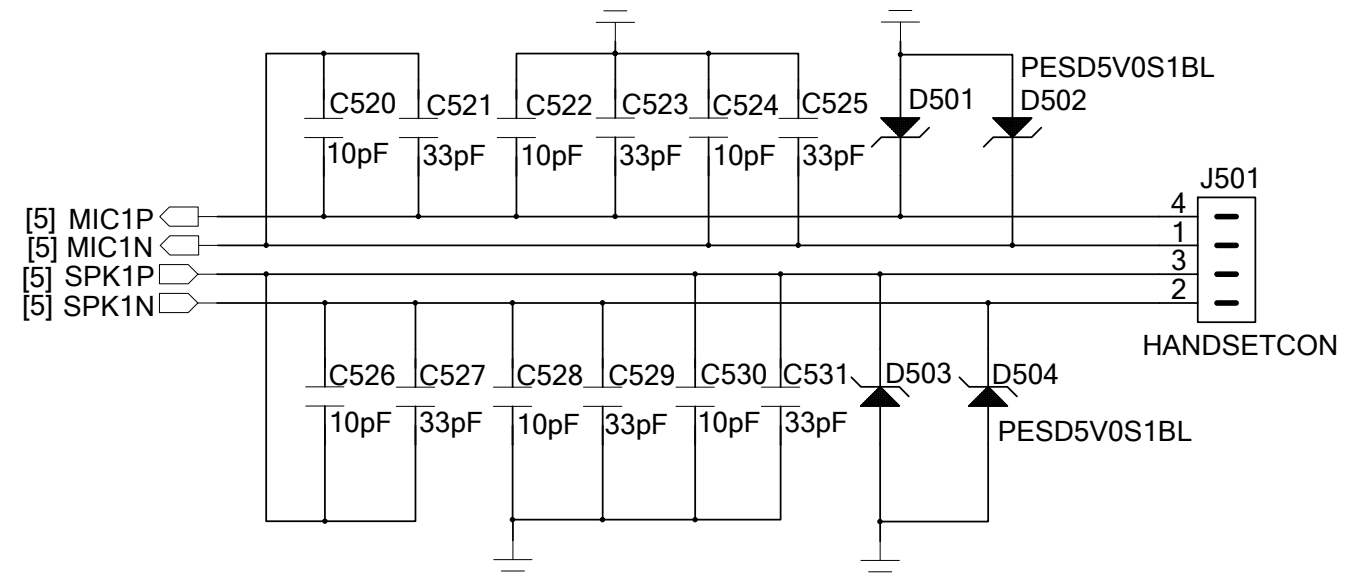
PCM Codec Circuit



Audio Channel - Earphone



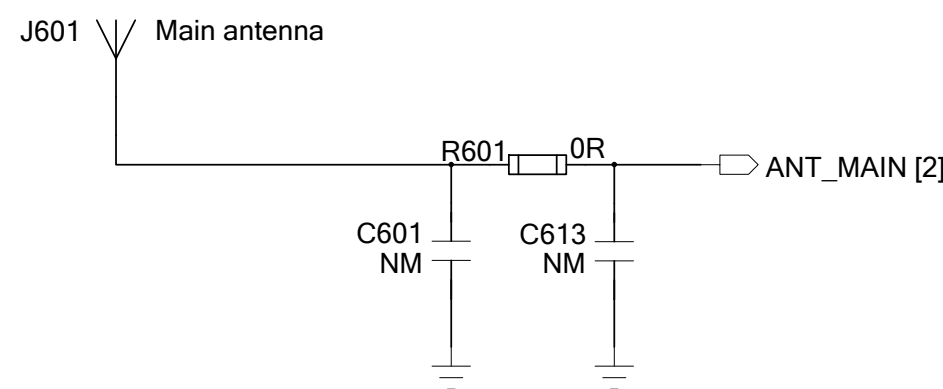
Audio Channel - Handset



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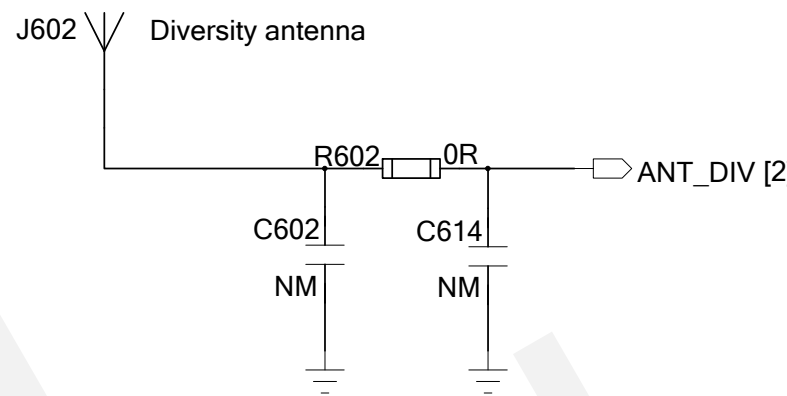
RF and GNSS Design

Main Antenna Interface



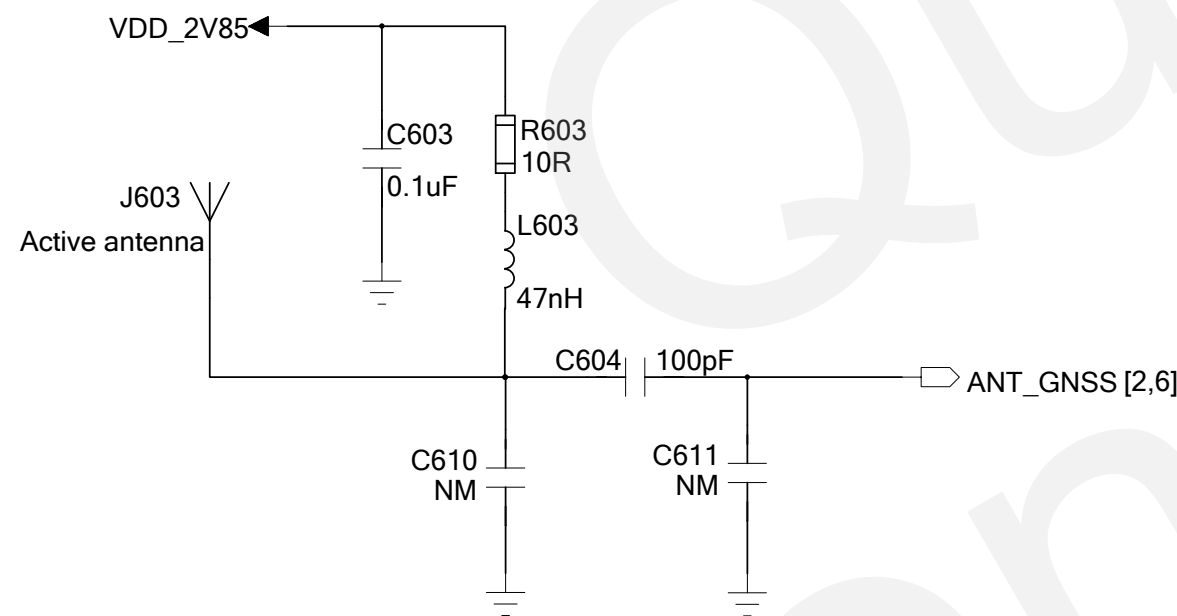
C601 and C613 are reserved for impedance matching.

Diversity Antenna Interface



ANT_DIV is used to improve UMTS receiving performance.

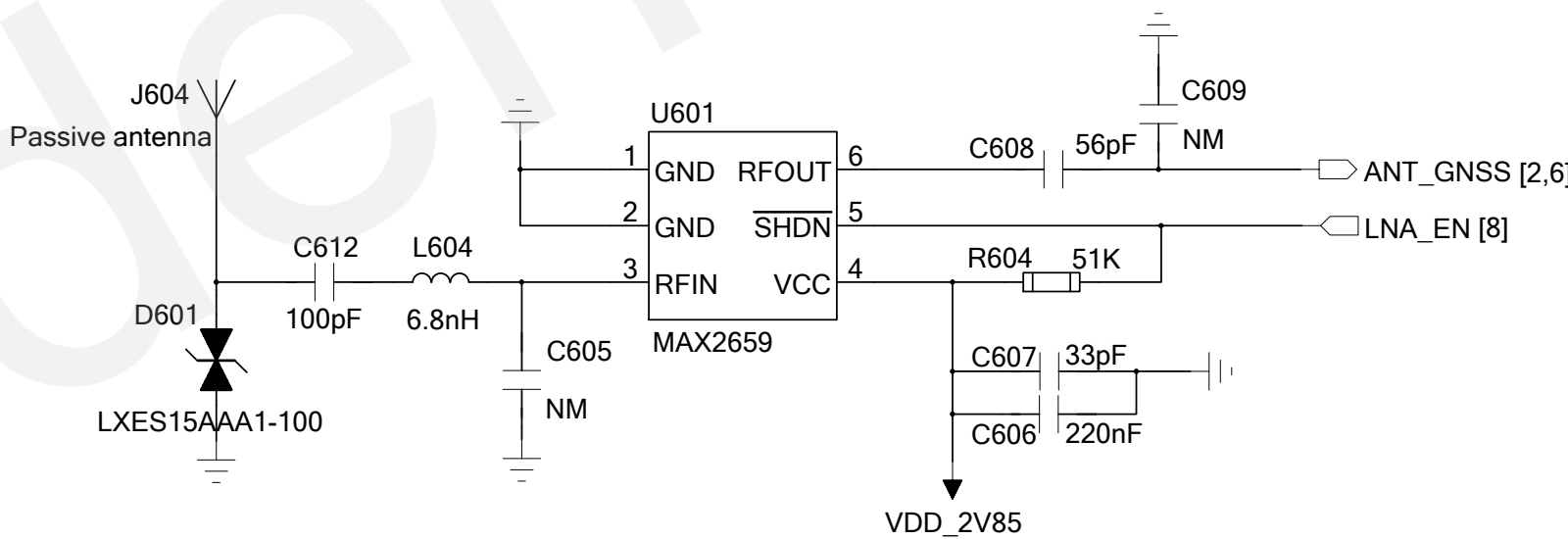
GNSS Active Antenna Circuit



Notes:

1. If customers design the antenna circuit with passive antenna, the R603 and L603 are not needed.
2. Customer can choose an external LDO to supply power to the active antenna, if VDD_2V85 cannot meet the power requirements of the active antenna.

GNSS Passive Antenna Circuit



Notes:

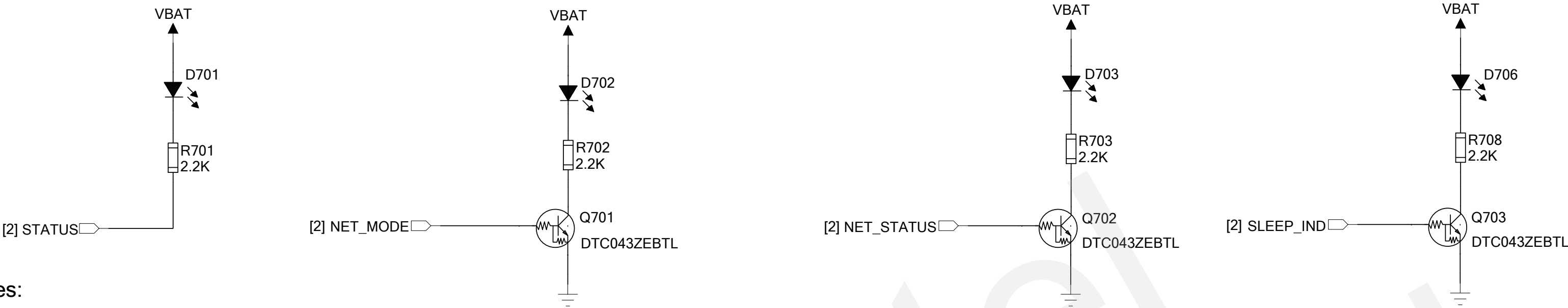
1. One typical reference circuit based on MAX2659 is shown above.
2. Customers can use one GPIO turning on and off the LNA U601.
3. The capacitance value of D601 should be less than 1pF.

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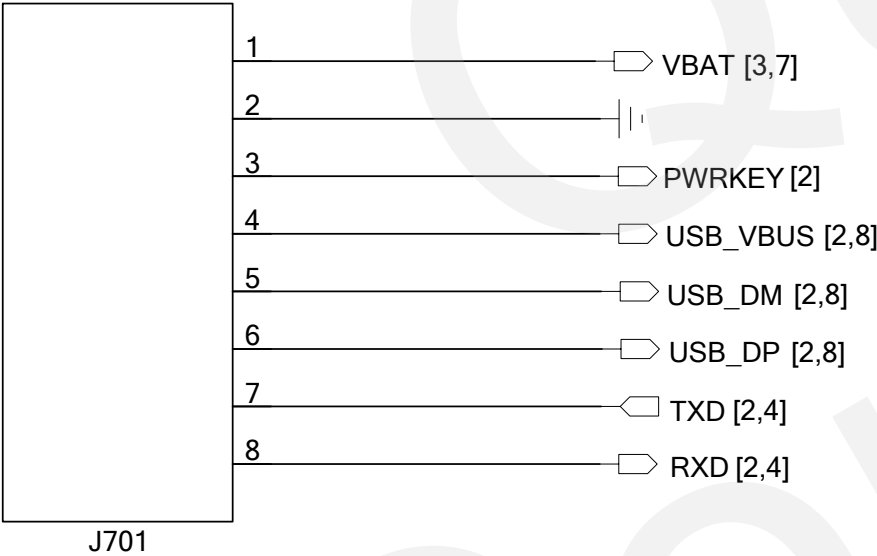
Other Designs

Indicators



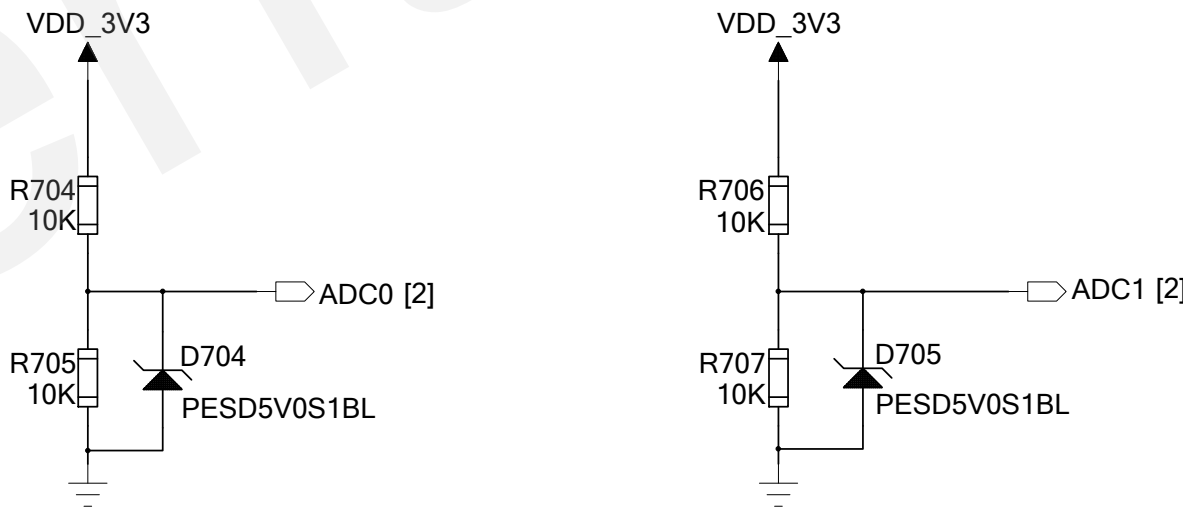
- Notes:
- 1. UC20 STATUS is open drain output.
 - 2. Refer to the document <UC20_Hardware_Design> for more details about NET_MODE, NET_STATUS and SLEEP_IND.

Reserved Testpoints



- Notes:
- 1. USB and UART interface are reserved for firmware upgrade, refer to the document <UC20_Hardware_Design> for details.
 - 2. It is recommended to add ESD protection components (e.g. ESDA6V8AV6) on these reserved testpoints. In addition, the ESD diodes used on USB data lines should have less than 2 pF of capacitance.

ADC Design



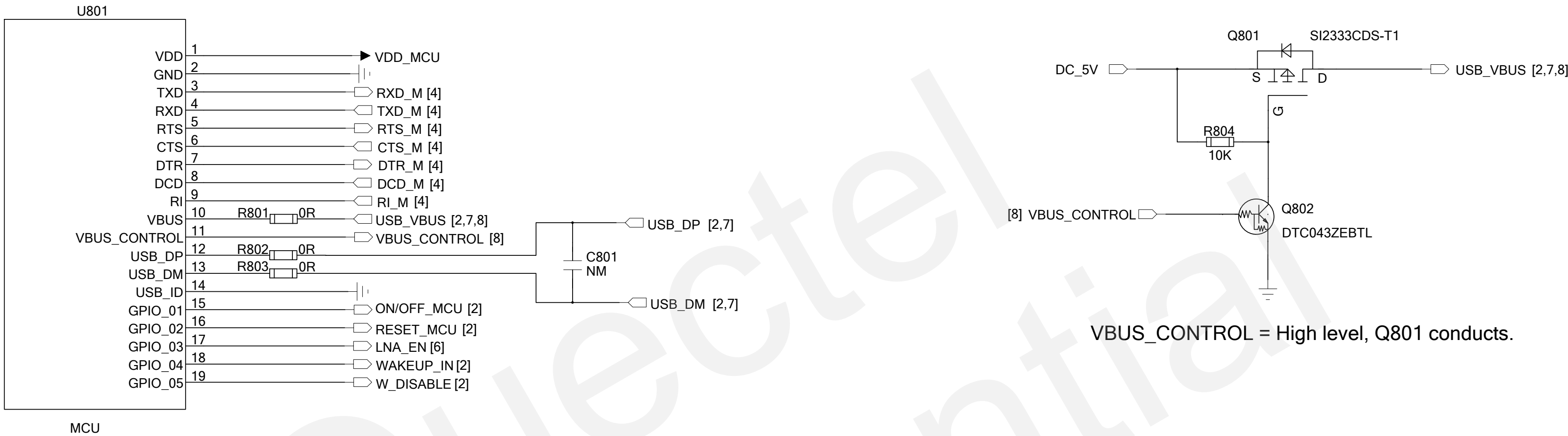
Note:

Input voltage range of ADC0 channel is 0.2~2.1V, and the ADC1 channel is 0.2~4.2V.

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MCU Interface



- Notes:
1. U801 represents customer's MCU.
 2. Pay attention to the UART connection of RTS/CTS.
 3. UC20 can only work as a USB device and supports FS/HS mode. To communicate with USB interface, MCU needs to support USB host or OTG function.
The VBUS pins of MCU and UC20 need to be provided 5V power for USB detection, and VBUS_CONTROL turns on and off VBUS power supply.
 4. Customers can determine to use USB or UART communication according to their needs.

Application	Installed	Not installed
USB	R801~R804, Q801~Q802	U401 circuit
UART	U401 circuit	R801~R804, Q801~Q802

5. Please pay attention to LNA_EN voltage level translation if the voltage domain of MCU is 5V.

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